A GaAs MHEMT Distributed Amplifier With 300-GHz Gain-Bandwidth Product for 40-Gb/s Optical Applications

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Abstract — **A distributed amplifier with greater than 13.4 dB gain and 65 GHz bandwidth has been demonstrated using 0.15 μm metamorphic GaAs HEMT technology. The amplifier has an average noise figure of 3.1 dB from 2-40 GHz and an output 1-dB compression point of 11 dBm at 22 GHz. The group delay variation from 1 to 40 GHz is ±7.5 ps. The amplifier may be biased with a single supply voltage, and consumes only 105 mW. With these characteristics, the amplifier is ideally suited for 40-Gb/s optical networks.**

I. Introduction

In the last few years many semiconductor manufacturers have aggressively developed products, including entire chipsets [1]-[4], for 40-Gb/s optical networks. The analog components for these high-speed transmit and receive modules must have uniform amplitude and phase response from kilohertz to gigahertz frequencies. Distributed amplifier (DA) circuits exhibit these features and have been the subject of many recent developmental efforts for 40-Gb/s systems. To date, DAs fabricated on InP substrates [5]-[9] have achieved higher gain-bandwidth products than those fabricated on GaAs [10]-[14]. However, metamorphic HEMTs (MHEMT) on GaAs substrates are more cost effective and manufacturable than devices on InP substrates[13]. We have demonstrated a MHEMT DA that rivals the gain-bandwidth product of similar InP designs.

This DA circuit is optimized to performance requirements that are critical for high-speed optical networks: low power dissipation, flat group delay and amplitude response, and operation from a single supply voltage. The DA has an output voltage capability of greater than 2 Vp-p into 50 Ω, and can be used after a transimpedance amplifier in a receiver circuit or as an amplification stage before a high-voltage driver in a transmitter.

II. Device Technology

Circuits were fabricated on 100 mm GaAs substrates using 0.15 μm T-gate MHEMT transistor technology [15]. The metamorphic HEMT layers were grown by molecular beam epitaxy (MBE). A major feature of this MHEMT technology is a composite InGaAs channel with an Indium mole fraction ranging from 53% to 63%. The transistor f_t is greater than 150 GHz after passivation steps are performed.

Typical maximum transconductance of 0.15 μm gate length MHEMT devices is 800 mS/mm at a drain voltage of 1.5 V. The average pinch-off voltage is –0.1 V with very good uniformity across the wafer. Gate to drain breakdown voltage is 5 V and maximum drain current density is greater than 500 mA/mm.

III. DA Circuit Design

The gain-bandwidth product of a DA is essentially a function of the device speed (f_t) at its intended bias. Gain and bandwidth are interchanged by the selection of cell size and the number of cells used in the distributed topology. For our gain and bandwidth target, series gate capacitor division [5],[6],[12] is not necessary due to the intrinsically high f_t of the MHEMT devices. This eliminates the need for series and shunt gate resistors to allow DC bias, which often come with a noise figure and low frequency gain flatness penalties. The bias and transistor periphery is selected by considering the needed output voltage swing. Our goal 1-dB compression point was 10 dBm, or 2 Vp-p into 50 Ω. A total transistor periphery of 0.56 mm was used.

A cascode cell was chosen for the DA instead of a single common-source (CS) transistor. This choice allows a larger output voltage swing than a single CS transistor at the same quiescent bias. Additionally, the CS FET of the cascode is biased at a low drain-source voltage in which the transconductance and gate capacitance is favorable, allowing for a large gain-bandwidth. The DA was designed using 7 cascode pairs as unit cells.

The circuit is most easily biased through gate and drain termination resistors. Contact pads are available for access to the gate of the CS device (V_{g1}), the gate of the common-gate (CG) device (V_{g2}), and the drain supply (V_{dd}). When biased through the termination resistors, V_{g1}, V_{g2} and V_{dd} are set to +0.3 V, +1.1 V, and +4.5 V, respectively. With these bias voltages, the drain current is

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42 mA. Resistor dividers are also included on-chip to provide bias to the DA with a single 4.5-V supply. The power consumption can be reduced to 105 mW by applying 2.5 V through a bias tee at the RF output pad. A circuit schematic and photograph of the 1.36 mm by 1.17 mm MMIC are shown in Figure 1.

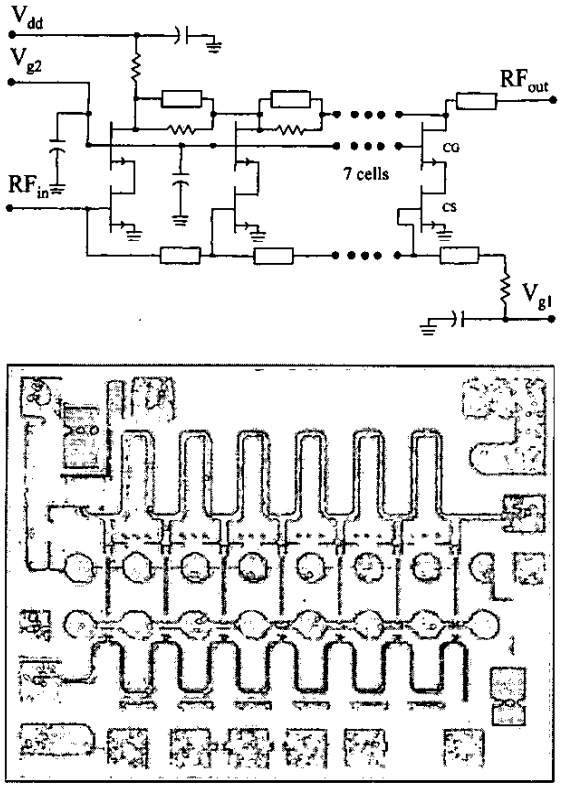

Fig. 1. Circuit schematic and photograph of the MHEMT distributed amplifier

Gain and group delay flatness were key considerations in the design of the DA, which result in low phase jitter and eye pattern signal-to-noise ratio. Additional amplitude flatness was achieved by connecting large resistors between the output of each cascode cell. These resistors tend to damp gain ripples at frequencies near the band edge and ensure stability beyond the cutoff frequency.

IV. Measured Results

For measurements of the DA circuits, the die were soldered to Cu-Mo carrier plates. The fixture includes 1.8 nF and 0.1 µF capacitors for bypassing the drain and gate lines. S-parameters were then measured at 45 MHz-110 GHz, with the reference plane at the center of the RF pads on the chip. The S-parameters from 45 MHz-80 GHz are shown in Figure 2. The bias was applied through tees in the network analyzer and an external needle probe. The mean value of the gain from 45 MHz-50 GHz is 14.5 dB. The 3-dB bandwidth is 65 GHz, using 14.5 dB for the midband gain. The gain flatness is ± 0.9 dB from 1-40 GHz. The input and output return losses are greater than 13 dB and 12 dB, respectively.

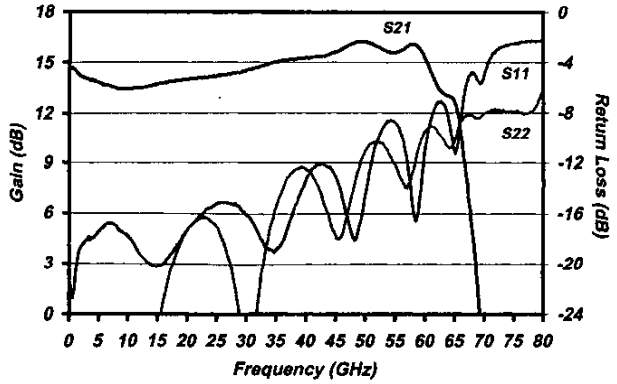

Fig. 2. Gain and return loss versus frequency

The group delay versus frequency from 1-60 GHz is shown in Figure 3. The S-parameters shown in Figure 2 were used for the group delay calculation. The group delay was calculated using a 2% aperture. The peak-to-peak variation is ±7.5 ps from 1-40 GHz. Low phase dispersion from this DA results in low additive jitter in a 40-Gb/s system.

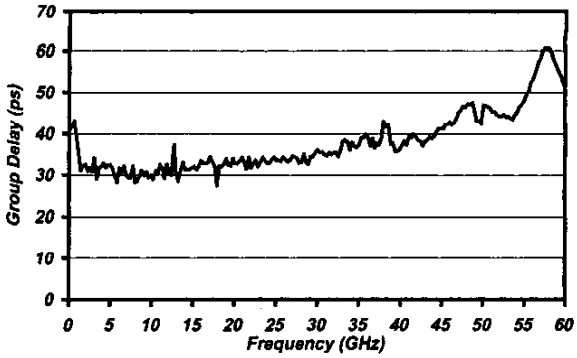

Fig. 3. Group delay versus frequency

For the remaining measurements in this paper, the circuits were bonded to 10-mil alumina substrates using 3 wires. The data was corrected for the loss in the microstrip lines on the alumina substrate. The output 1-dB compression point (P_{1dB}) is shown versus frequency from

2-50 GHz in Figure 4. With a bias of 4.5 V and 42 mA, the P_{1dB} is greater than 10 dBm from 2-20 GHz. When the drain bias is raised to 6 V and 52 mA, the resulting P_{1dB} at 22 GHz is 13.7 dBm. For this bias condition, V_{g2} was raised to 1.75 V.

Also shown in Figure 4 is the 50 Ω noise figure of the DA at a bias of 4.5 V and 42 mA. The noise figure was obtained for 2-40 GHz using a separate sweep from 2-26 GHz and 27-40 GHz. The average noise figure is 3.1 dB over the entire band. The rise in noise figure at low frequencies is due to the contribution of the gate termination resistor.

Output power and gain versus input power at 22 GHz are plotted to show the compression characteristic of the DA. The result of biasing the DA at the 4.5 V and 6 V conditions described above is compared in Figure 5. The DA can deliver 2 Vp-p wideband signals into 50 Ω. Furthermore, there is no evidence of gain expansion at low input power levels.

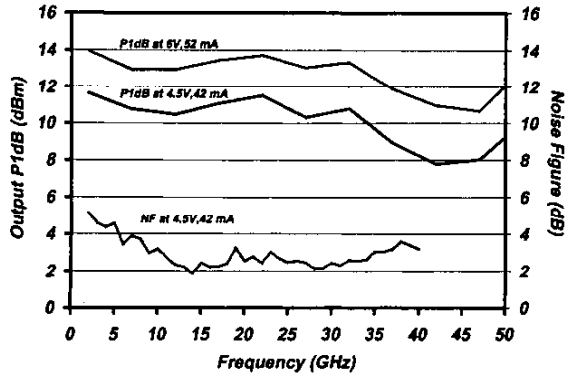

Fig. 4. Output P_{1dB} and noise figure versus frequency

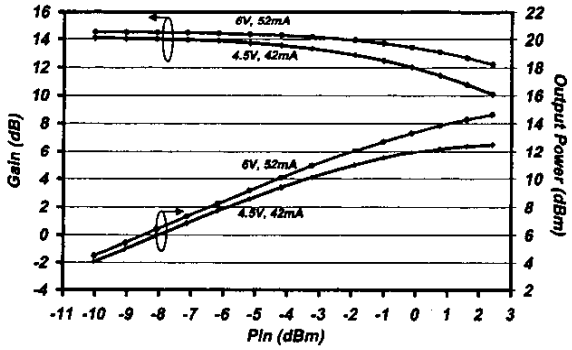

Fig. 5. Output power and gain versus input power at 22 GHz

To show that the DA is capable of amplifying wideband data streams at 40 Gb/s, a pseudo-random data sequence with a word length of 2^{31}-1 was applied to the chip. The resulting output eye pattern at the output is shown in Figure 6. The pattern shows a wide opening with low jitter and 438 mV between peak 0 and 1 levels. The input level for this measurement was 90 mVp-p, neglecting loss in the alumina lines and microstrip to coax transitions.

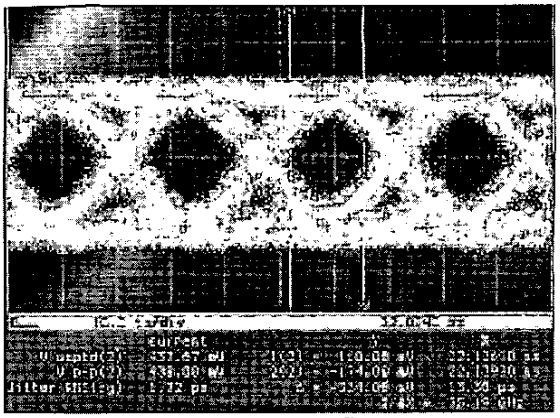

Fig. 6. Output of DA with 40 Gb/s 2^{31}-1 PBRS input

The RF performance of each DA circuit was tested at TriQuint's production facility. A histogram of the of the gain at 40 GHz across an entire 100 mm wafer is shown in Figure 7. Over 50% of the 468 circuits have gain within 0.15 dB of the mean gain value of 15.1 dB. This result highlights the excellent uniformity of TriQuint's 0.15 µm MHEMT process.

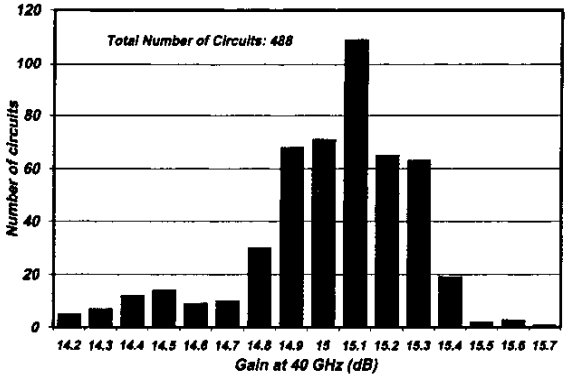

Fig. 7. Histogram of gain at 40 GHz for a wafer.

V. SUMMARY

A 0.15 µm MHEMT distributed amplifier, that is well suited to the stringent demands of high-speed optical networks, has been demonstrated. The performance of this MHEMT DA circuit is repeatable and competitive with similar InP designs. The DA, which has voltage gain

greater than 4.5 V/V, drive capability greater than 2 Vp-p, and bandwidth greater than 50 GHz, is a versatile element for both optical receivers and transmitters. The low power dissipation, single supply bias option, and compact chip size allow for simpler high-speed modules and can help to drive the market for 40-Gb/s networks.

ACKNOWLEDGEMENTS

Craig Steinbeiser and Thomas Landon performed the 40-Gb/s eye pattern measurements. The authors would like to thank Qingmin Liu of Notre Dame University for assistance with the S-parameter measurements and Alan Seabaugh of Notre Dame University for the use of the Agilent 8510XF network analyzer.

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